IN THE SPECIFICATION:

Paragraph beginning at line 24 of page 9 has been amended as follows:

The amplification unit 3 may be constituted by a MOS source follower, a voltage follower amplifier or the like and may also be provided with an amplifier enable terminal 10 through which an operation state is selected. In addition, a parasitic ~~capacity~~ capacitor 9 exists between a gate and a source of the MOS transistor 6.

Paragraph beginning at line 21 of page 10 has been amended as follows:

Thus, as shown in FIG. 2, after the reset switch 2 is turned OFF in accordance with ΦR(n), the transfer switch 4 is turned ON in accordance with ΦT1(n) to read out the reference signal to the ~~capacity~~ capacitor 5 for a time interval TR. The reference signal is held in the ~~capacity~~ capacitor 5 for one period. For this time interval, the photocharges are accumulated in the photodiode 1, and the electric potential appearing at the output terminal Vdi fluctuates in correspondence to a quantity of photocharges. At the time when the channel selection switch 7 is turned ON in accordance with ΦSCH(n) of the next period, the reference

signal held in the capacity 5 is read out to the common signal line 11 for a time interval REF. Next, if ΦT1(n) is turned ON to read out an optical signal corresponding to a quantity of electric charges accumulated in the photodiode 1 to the capacitor 5 for a time interval TS, then this optical signal is read out to the common signal line 11. If ΦT1(n) is turned ON, then the optical signal is accumulated in the capacitor 5. However, if for the time interval TS when ΦT1(n) is held in an ON state, a drivability of the amplification unit 3 is set so that settling for an electric potential appearing at a terminal V1 is obtained, then a time interval when ΦSCH(n) is held in an ON state can be shortened to allow a high speed operation to be carried out.

Paragraph beginning at line 22 of page 13 has been amended as follows:

Thus, as shown in FIG. 5, after the reset switch 2 is turned OFF in accordance with ΦR(n), the transfer switch 4 is turned ON in accordance with ΦT1(n) to read out the reference signal to the capacity 5 for a time interval TR. At this time, the second current source 51 is turned ON in accordance with an enable signal ΦRR(n). The reference signal is held in the ~~capacity~~ capacitor 5 for one period. For this time interval, the photocharges are accumulated in the

photodiode 1, and the electric potential appearing at the output terminal Vdi fluctuates in correspondence to a quantity of photocharges. At the time when the channel selection switch 7 is turned ON in accordance with ΦSCH(n) of the next period, the reference signal held in the ~~capacity~~ capacitor 5 is read out to the common signal line 11 for a time interval REF. Next, if ΦT1(n) is turned ON to read out an optical signal to the capacitor 5, this optical signal is read out to the common signal line 11.

Paragraph beginning at line 13 of page 14 has been amended as follows:

At this time, the first current source 8 is turned ON, while the second current source 51 is turned OFF. The first current source 8 and the second current source 51 are designed so as to cause substantially the same ON-current to flow therethrough. Thus, an electric potential appearing at a source electrode of the MOS transistor 6 when the reference signal is read out to the capacitor ~~23~~ 5 for a time interval R1 can be made substantially the same as that when the optical signal is read out to the capacitor ~~23~~ 5 for a time interval S1. Consequently, it is possible to reduce an influence of the parasitic ~~capacity~~ capacitor 9 on the electric charges accumulated in the capacitor 5, which results in that an offset of a dark output voltage can be made small.

Paragraph beginning at line 17 of page 18 has been amended as follows:

The circuit of this embodiment includes: the photodiode 1 serving as a photoelectric conversion unit; transfer switches 18, 19 and 20 each serving as an electric charge transfer unit; a reset switch 2 serving as a reset unit; amplification units 15, 16 and 17; capacitors 21, 22 and 23; the MOS transistor 6 constituting a MOS source follower; the channel selection switch 7 serving as a channel selection unit; the common signal line 11; and the first current source 8. The amplification units 15,16 and 17 maybe each constituted by a MOS source follower, a voltage follower amplifier, or the like, and may also be provided with amplifier enable terminals 12, 13 and 14 for selection of operation states, respectively. In addition, the parasitic ~~capacity~~ capacitor 9 exists between a gate and a source of the MOS transistor 6.

Paragraph beginning at line 13 of page 26 has been amended as follows:

The circuit of this embodiment includes: the photodiode 1 serving as a photoelectric conversion unit; the transfer switches 18, 19 and 20 each serving as an electric charge transfer unit; the reset switch 2 serving as a reset

unit; the amplification units 15, 16 and 17; the capacitors 21, 22 and 23; the MOS transistor 6 constituting a MOS source follower; a second current source connected to a source of the MOS transistor 6; the channel selection switch 7 serving as a channel selection unit; the common signal line 11; and the first current source 8. The amplification units 15, 16 and 17 may be each constituted by a MOS source follower, a voltage follower amplifier or the like, and may also be provided with the amplifier enable terminals 12, 13 and 14 for selection of operation states, respectively. In addition, the parasitic ~~capacity~~ capacitor 9 exists between a gate and a source of the MOS transistor 6.

Paragraph beginning at line 2 of page 30 has been amended as follows:

At this time, the first current source 8 is turned ON, while the second current source 51 is turned OFF. The first current source 8 and the second current source 51 are designed so as to cause substantially the same ON-current to flow therethrough. Thus, an electric potential appearing at a source electrode of the MOS transistor 6 when the reference signal is read out to the capacitor 23 for a time interval R1 can be made substantially the same as that when the optical signal is read out to the capacitor 23 for a time interval S1.

Consequently, it is possible to reduce an influence of the parasitic ~~capacity~~ capacitor 9 on the electric charges accumulated in the capacitor 23, which results in that an offset of a dark output voltage can be made small.